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TITLE: Genus tower light controller

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INVENTOR-INFORMATION:

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US-CL-CURRENT: 340/635; 340/634

CLAIMS:

I claim:

1. An apparatus for indicating the states of a semiconductor **wafer** production process, comprising:

cassette logic circuitry for generating a first signal that varies depending upon whether **wafers** are present in a chamber or if said chamber is empty and depending upon whether said chamber is at atmospheric pressure or if said chamber is pumped down to a vacuum;

first indicator logic circuitry, connected to said cassette logic circuitry, for receiving said first signal, for continuously driving a first indicator when said chamber is ready to be loaded with **wafers**, and for intermittently driving said first indicator when said first signal indicates that said chamber has **wafers** that are ready to be unloaded;

second indicator logic circuitry for intermittently driving a second indicator when an alarm signal is received and for continuously driving said second indicator when said production process is placed in an interrupt mode; and

third indicator logic circuitry for continuously driving a third indicator when **wafers** in said chamber are being processed;

wherein said second indicator logic circuitry is connected to said first indicator logic circuitry and to said third indicator logic circuitry and prevents said first

indicator logic circuitry and said third indicator logic circuitry from respectively
driving said first and third indicators whenever said alarm signal is received at
said second indicator logic circuitry.

2. An apparatus as set forth in claim 1, wherein:

said cassette logic circuitry is also for generating a second signal that varies
depending upon whether **wafers** are present in a second chamber or if said second
chamber is empty and depending upon whether said second chamber is at atmospheric
pressure or if said second chamber is pumped down to a vacuum; and

said first indicator logic circuitry is also for receiving said second signal and
for continuously driving said first indicator when said second chamber is ready to
be loaded with **wafers,** and for intermittently driving said first indicator when said
first signal indicates that said second chamber has **wafers** that are ready to be
unloaded.

3. An apparatus as set forth in claim 2, wherein said cassette logic circuitry
comprises:

a first JK flip-flop for receiving a first atmosphere signal at its clock input and
a first cassette present signal at its clear input and for outputting said first
signal at its Q output; and

a second JK flip-flop for receiving a second atmosphere signal at its clock input
and a second cassette present signal at its clear input and for outputting said
second signal at its Q output.

4. An apparatus as set forth in claim 3, wherein said first indicator logic
circuitry comprises:

an OR gate having said first signal and said second signal as inputs; and

means for transmitting an oscillating signal to said first indicator for flashing
said first indicator when an output of said OR gate is at a logical value of "1" and
for transmitting a constant voltage signal for continuously driving said first
indicator when said output of said 0R gate is at a logical value of "0."

5. An apparatus as set forth in claim 2, wherein said first indicator logic circuitry comprises:

a first AND gate having a first cassette present signal and a first atmosphere signal as inputs;

a second AND gate having a second cassette present signal and a second atmosphere signal as inputs;

a third AND gate having outputs from said first AND gate and second AND gate as inputs; and

means for receiving an output of said third AND gate and for turning off said third indicator when said output of said third AND gate is at a logical value of "1."

6. An apparatus as set forth in claim 2, wherein said second indicator logic circuitry comprises:

a first switch for transmitting an oscillating signal to said second indicator for flashing said second indicator when said alarm signal is at a logical value of "1"; and

a second switch for transmitting a constant voltage signal to said second indicator for continuously driving said second indicator when said second switch is closed during said interrupt mode.

7. An apparatus as set forth in claim 1, wherein said first indicator is a yellow lamp, said second indicator is a red lamp, and said third indicator is a green lamp.

8. An apparatus as set forth in claim 1, wherein said third indicator logic circuitry comprises a switch for receiving a process signal at an input and an inverted alarm signal at a control gate and for passing said process signal through to a relay and to said third indicator whenever said inverted alarm signal is not received at said control gate.

9. An apparatus as set forth in claim 1, further comprising means for generating an oscillating signal that is used by said first indicator logic circuitry for intermittently driving said first indicator and by second logic indicator circuitry

for intermittently driving said second indicator.

10. An apparatus for indicating the states of a semiconductor **wafer** production process, comprising:

cassette logic circuitry for generating a first signal that varies depending upon whether **wafers** are present in a chamber or if said chamber is empty and depending upon whether said chamber is at atmospheric pressure or if said chamber is pumped down to a vacuum;

first indicator logic circuitry, connected to said cassette logic circuitry, for receiving said first signal, for continuously driving a first indicator when said chamber is ready to be loaded with **wafers,** and for intermittently driving said first indicator when said first signal indicates that said chamber has **wafers** that are ready to be unloaded;

second indicator logic circuitry for intermittently driving a second indicator when an alarm signal is received and for continuously driving said second indicator when said production process is placed in an interrupt mode;

third indicator logic circuitry for continuously driving a third indicator when **wafers** in said chamber are being processed; and

means for generating an oscillating signal that is used by said first indicator logic circuitry for intermittently driving said first indicator and by said second indicator logic circuitry for intermittently driving said second indicator;

wherein said second indicator logic circuitry is connected to said first indicator logic circuitry and to said third indicator logic circuitry and prevents said first indicator logic circuitry and said third indicator logic circuitry from respectively driving said first and third indicators whenever said alarm signal is received at said second indicator logic circuitry.

11. An apparatus for indicating the states of a semiconductor **wafer** production process, comprising:

cassette logic circuitry for generating a first signal that varies depending upon whether **wafers** are present in a chamber or if said chamber is empty and

depending
whether said chamber is at atmospheric pressure or if said chamber is pumped down to
a vacuum;

first indicator logic circuitry, connected to said cassette logic circuitry, for
receiving said first signal, for continuously driving a first indicator when said
chamber is ready to be loaded with **wafers**, and for intermittently driving said first
indicator when said first signal indicates that said chamber has **wafers** that are
ready to be unloaded;

second indicator logic circuitry for intermittently driving a second indicator when
an alarm signal is received and for continuously driving said second indicator when
said production process is placed in an interrupt mode;

third indicator logic circuitry for continuously driving a third indicator when
wafers in said chamber are being processed; and

means for generating an oscillating signal that is used by said first indicator
logic circuitry for intermittently driving said first indicator and by said second
logic indicator circuitry for intermittently driving said second indicator, said
oscillating signal generating means comprising:

a first inverter, a second inverter, and a third inverter connected in series with
each other;

a first resistor and a second resistor connected in series with each other and
between said first inverter and said third inverter;

a capacitor having a first terminal connected between said second inverter and said
third inverter and a second terminal connected between said first resistor and said
second resistor;

a first **LED** connected across said second inverter; and

a second **LED** connected across said second inverter and being reverse biased with
respect to said first **LED**;

wherein said oscillating signal is generated at an output of said third inverter and
said first **LED** and said second **LED** enable said oscillating signal to have a lower

frequency than that possible without said first LED and said second LED;

wherein said second indicator logic circuitry is connected to said first indicator logic circuitry and to said third indicator logic circuitry and prevents said first indicator logic circuitry and said third indicator logic circuitry from respectively driving said first and third indicators whenever said alarm signal is received at said second indicator logic circuitry.

12. An apparatus for generating an oscillating signal, comprising:

a first inverter, a second inverter, and a third inverter connected in series with each other;

a first resistor and a second resistor connected in series with each other and between said first inverter and said third inverter;

a capacitor having a first terminal connected between said second inverter and said third inverter and a second terminal connected between said first resistor and said second resistor;

a first LED connected across said second inverter; and

a second LED connected across said second inverter and being reverse biased with respect to said first LED;

wherein said oscillating signal is generated at an output of said third inverter and said first LED and said second LED enable said oscillating signal to have a lower frequency than that possible without said first LED and said second LED.